C1 AM cont'd

initiating said refresh during a time period between said first predetermined time slot and a second predetermined time slot without delaying said data access.

4. (Amended) The method of claim 1 further comprising determining whether said data access command conflicts with said refresh.

C1 A2

8. (Amended) The method of claim 7 further comprising:

determining that a second data access command has been applied to said command/address bus at said next available time slot; and

determining whether said second data access command conflicts with said refresh.

C1 A3

13. (Amended) A system for refreshing memory cells of a dynamic random access memory (DRAM) comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

35. (Amended) An integrated circuit semiconductor device containing a system for refreshing memory cells of a dynamic random access memory (DRAM), said integrated circuit semiconductor device comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

45. (Amended) A processor-based system, comprising:

a processor; and

a dynamic random access memory (DRAM) coupled to said processor, said dynamic random access memory having a system for refreshing memory cells in said dynamic random access memory, said system comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for operating said memory array in accordance with said data access commands, wherein

said controller is configured to determine that said memory cells require a refresh, and wherein

said controller is configured to initiate said refresh at a predetermined time and without delaying a data access triggered by a data access command.

52. (Amended) The processor-based system of claim 51, wherein said predetermined edge is defined as every fourth positive edge of a dynamic random access memory (DRAM) input clock.

Add new claims 55-58 as follows.

55. A method for refreshing memory cells, comprising:

assigning predetermined time slots during which a data access command may be placed on a command/address bus; and

performing a non-conflicting refresh operation during a period of time between said predetermined time slots.

56. A system for refreshing memory cells of a dynamic random access memory (DRAM) comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for performing a non-conflicting refresh on said memory cells during a time interval between said predetermined time slots.

57. An integrated circuit semiconductor device containing a system for refreshing memory cells of a dynamic random access memory (DRAM), said integrated circuit semiconductor device comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for performing a non-conflicting refresh on said memory cells during a time interval between said predetermined time slots.

58. A processor system, comprising:

a processor unit; and

a dynamic random access memory (DRAM) coupled to said processor, said dynamic random access memory having a system for refreshing memory cells in said dynamic random access memory, said system comprising:

a memory array containing said memory cells;

a communication link for delivering data access commands to said DRAM on predetermined time slots; and

a controller for performing a non-conflicting refresh on said memory cells during a time interval between said predetermined time slots.